The Examiner has rejected Claims 33 and 35-37 under 35 U.S.C. §102(b) as being clearly anticipated by Vo (U.S. Patent No. 5,097,381), and has also rejected Claim 34 as being obvious over Vo and a secondary reference. In particular, the Examiner points to column 5, lines 20-45, teaching a trench with an aspect ratio greater than about 20:1, a dielectric layer 45 lining the trench and a conductively doped polysilicon layer 52 filling the trench.

Applicants have amended Claim 33 to recite the doped silicon that fills the trench to comprise "as-deposited polysilicon." Applicants submit that the amendment is fully supported by the application as filed and introduces no new matter. For example, page 14, line 35 to page 15, line 2 indicates that polysilicon is formed at temperatures greater than or equal to about 650°C (compared to amorphous silicon at lower temperatures), and the data in Table II of the present application as filed (pages 20-22) shows that silicon can be deposited by the preferred embodiments at the temperature ranges for polysilicon with extremely high step coverage into narrow holes.

Applicants respectfully submit that as-deposited polysilicon is ***structurally distinct*** from silicon deposited as amorphous silicon (α-Si) and annealed to form polycrystalline silicon. For example, provided in a Supplemental Information Disclosure Statement (IDS) herewith is an article by R. Kakkad et al., "Crystallized Si Films By Low-Temperature Rapid Thermal Annealing Of Amorphous Silicon," J.Appl. Phys., Vol. 65, No. 5 (March 1, 1989), pp. 2069-2072. This article indicates the known structural distinctions between polysilicon that is formed by direct polysilicon deposition and polysilicon that is formed by depositing amorphous silicon and then annealing. For example, the abstract of that article states "Unlike deposited polycrystalline Si films, the grain size in these crystallized films is not limited by film thickness." Table II (p. 2071, second column) of the article illustrates that amorphous silicon that is annealed to crystallize, has a conductivity of 160 S/cm, whereas directly deposited polysilicon with exactly the same doping concentration has a conductivity of 500 S/cm.

Accordingly, Applicants respectfully submit that the processes disclosed in the present application enable in-situ doped, as-deposited polysilicon with extremely high step coverage. In comparison, the cited reference Vo does not indicate any manner of processing and does not specify the nature of the polycrystalline film filling the disclosed narrow, deep holes.

Accordingly, the Applicants respectfully submit that the art of record does not teach or suggest the invention of independent Claim 33 as recited. The secondary reference and other art of record do not supply the deficiencies of Vo.

While Applicants have not separately addressed the rejections of the dependent claims as being moot in view of the amendments and remarks presented herewith, Applicants expressly do not acquiesce in the Examiner's findings with respect to the dependent claims, but decline to separately address them as moot in view of the amendments and remarks herein.

CONCLUSIONS

In view of the forgoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance and respectfully request the same. If, however, some issue remains that the Examiner feels can be addressed by Examiner's Amendment, the Examiner is cordially invited to call the undersigned for authorization.

The amendments are shown in marked up form in the attached separate pages entitled "**VERSION SHOWING CHANGES MADE TO THE CLAIMS**," in which deletions are shown ~~stricken through~~ and additions are shown in double-underlining.

Respectfully submitted,

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VERSION SHOWING CHANGES MADE TO THE CLAIMS

Claim 33 has been amended as indicated below.

33. (Amended) An integrated capacitor formed in a trench having a width of no more than about 0.25 μm and an aspect ratio greater than about 20:1, comprising:

a dielectric layer lining the trench; and

a conductively doped, as-deposited polysilicon layer filling the trench.

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